Nexolight

Datasheet

NXDA-PP-2M

SFP+ 10GBASE-CR 2m DAC Twinax

Features

- SFP+ Form Factor
- 10 Gb/s bitrate
- Up to 2 m over DAC Twinax
- Up to 1W power consumption
- +0/+70°C temperature range
- Built in digital diagnostic monitoring

Applications

- 10G Ethernet
- Serial Data Transmission

Recommended operating conditions

Parameter	Value	Unit
Storage temperature	-40/+85	°C
Operating case temperature	+0/+70	°C
Power supply voltage	3.3	V
Power consumption	1	W

Regulatory Compliance

- ESD to the Electrical PINs: compatible with MIL-STD-883 Method 3015.
- ESD to the Duplex LC Receptacle: compatible with IEC 61000-4-2.
- Immunity: compatible with IEC 61000-4-3.
- EMI: compatible with FCC Part 15 Class B EN55022 Class B (CISPR 22B) VCCI Class B.
- Laser Eye Safety: compatible with FDA 21CFR 1040.10 and 1040.11 EN60950, EN (IEC) 60825-1, 2.
- RoHS: compliant with 2002/95/EC 4.1&4.2 2005/747/EC.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Storage Temperature	Tstg	-40		85	°C
Operating Case Temperature	Tc	0		70	°C
Humidity	RH	5		85	%
Data Rate			10		Gbps

Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Length	L			2	M
AWG				30	AWG
Jacket Material	LSZH, Black				

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Resistance	Rcon			3	Ω
Insulation Resistance	Rins			10	MΩ
Raw Cable Impedance	Zca	95	100	110	Ω
Mated Connector Impedance	Zmated	85	100	110	Ω
Insertion Loss at 12.89GHz	SDD21			17.04	dB
Return Loss at 12.89GHz	SDD11/22	$\text{Return\_Loss(f)} \geq \begin{cases} 12 - 2\sqrt{f}, & 0.05 \leq f < 4.1 \\ 6.3 - 13\log 10\left(\frac{f}{5.5}\right), & 4.1 \leq f \leq 10 \end{cases}$			dB
Rise Time (20-80%)				34	ps

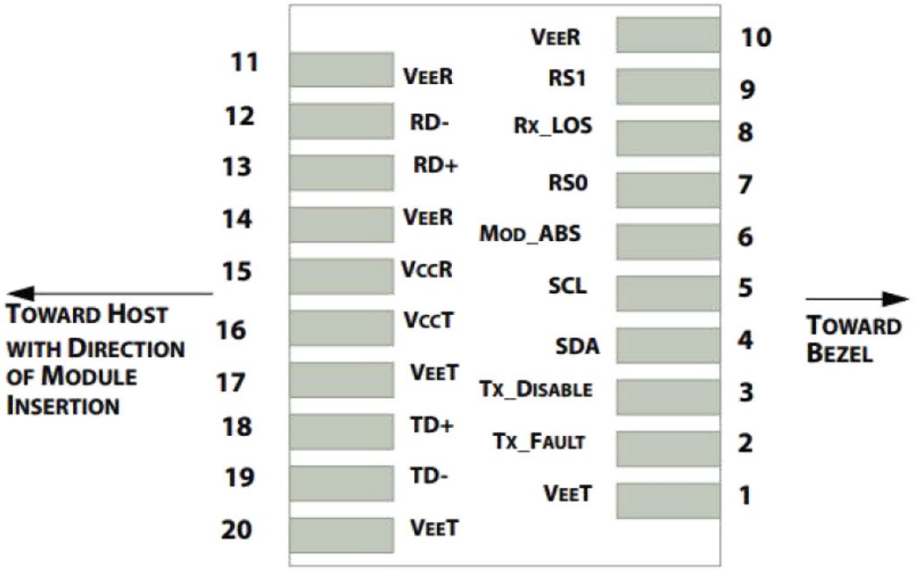
Pin Descriptions

Pin	Logic	Symbol	Name/Description	Plug Sequence	Note
1		VeeT	Module Transmitter Ground.	1	3
2	LVTTL-O	Tx_Fault	Module Transmitter Fault.	3	4
3	LVTTL-I	Tx_Disable	Transmitter Disable. Turns off transmitter laser output.	3	5
4	LVTTL-I/O	SDA	2-Wire Serial Interface Data. Same as MOD_DEF2 in INF-8074i.	3	
5	LVTTL-I/O	SCL	2-Wire Serial Interface Clock. Same as MOD_DEF1 in INF-8074i.	3	
6		MOD_ABS	Module Absent. Connected to VeeT or VeeR in the module.	3	
7	LVTTL-I	RS0	Rate Select 0. Optionally controls the SFP+ module receiver.	3	6
8	LVTTL-O	Rx_LOS	Receiver Loss of Signal indication. In FC, designated as Rx_LOS. In Ethernet, designated as Signal Detect.	3	4
9	LVTTL-I	RS1	Rate Select 1. Optionally controls SFP+ module transmitter.	3	6
10		VeeR	Module Receiver Ground.	1	3
11		VeeR	Module Receiver Ground.	1	3
12	CML-O	RD-	Receiver Inverted Data Output.	3	
13	CML-O	RD+	Receiver Non-Inverted Data Output.	3	
14		VeeR	Module Receiver Ground.	1	3
15		VccR	Module Receiver 3.3V Supply.	2	
16		VccT	Module Transmitter 3.3V Supply.	2	
17		VeeT	Module Transmitter Ground.	1	3
18	CML-I	TD+	Transmitter Non-Inverted Data Input.	3	
19	CML-I	TD-	Transmitter Inverted Data Input.	3	
20		VeeT	Module Transmitter Ground.	1	3

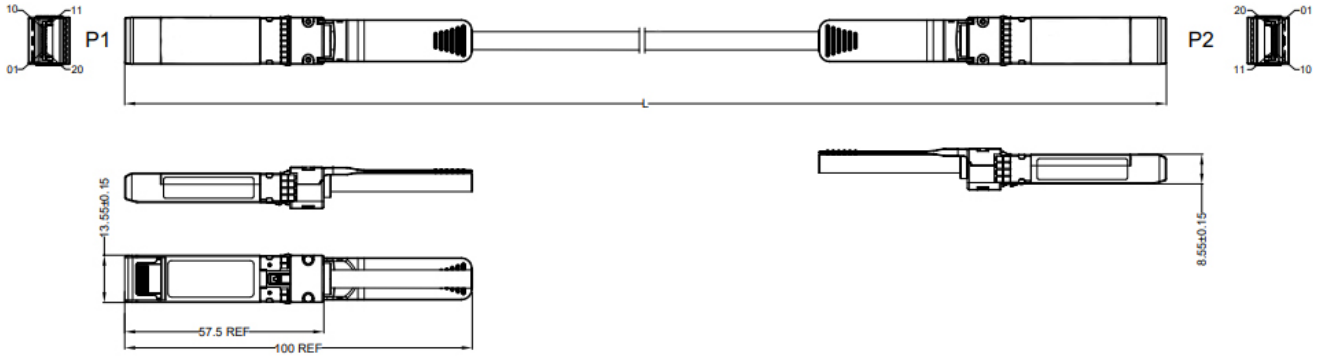
Notes:

1. Labeling as inputs (I) and outputs (O) are from the perspective of the module.
2. The case makes electrical contact to the cage before any of the board edge contacts are made.
3. The module signal ground contacts, VeeR and VeeT, should be isolated from the module case.
4. This contact is an open collector/drain output contact and shall be pulled up on the host. Pull-ups can be connected to one of several power supplies; however, the host board design shall ensure that no module contact has a voltage exceeding module VccT/R+0.5V.
5. Tx_Disable is an input contact with a 4.7kΩ to 10kΩ pull-up to the VccT inside the module.
6. If implementing SFF-8079, contacts 7 and 9 in SFF-8431 are used for AS0 and AS1, respectively.

Electrical Pin-Out Details



Mechanical Specifications



Notes:

1. 2 pairs.
2. 100% conductor test conditions: 5V, insulation resistance of 10MΩ, and conduction resistance maximum of 3Ω.